AN FM TUNER USING MOS-FET'S AND INTEGRATED CIRCUITS

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INTRODUCTION

The increasingly important role of the FM receiver in the consumer entertainment industry makes it a logical choice for introducing new semiconductor devices. The objective of the work described in this paper has been to develop a quality FM tuner incorporating new devices where they would result in improved performance and/or lower cost. MOS-FET r-f amplifier and integrated circuit i-f amplifier devices which are described are not laboratory curiousities but could be placed in production in the near future.

FM FRONT END

The FM front end shown in Fig. 1 uses a developmental N-Channel MOS-FET in the r-f amplifier and bipolar silicon Planar* transistors for the mixer and local oscillator. The front-end gain, which is 30 db, has been intentionally made low to increase the tuner overload capabilities without using AGC and to improve its spurious response rejection.[1]

The balanced 300-Ω input is transformed up to the gate of the neutralized common-source amplifier, Q_1. The depletion type N-Channel MOS-FET uses self-bias identical to cathode-bias commonly used in vacuum-tube amplifiers. In this amplifier, Q_1 is biased at 2 mA and 17 volts. At these conditions, the device has a noise figure of 3 db and can provide over 20-db gain at 100 Mc. However, the r-f stage gain is limited to 13 db by the 100-Ω resistor in the interstage transformer to prevent mixer overload. The resistor also presents the mixer transistor with a constant source conductance over the tuning range, which is important to having high spurious rejection in the mixer stage. The r-f gain of 13 db is sufficient to mask the noise generated by the mixer.

The mixer transistor, Q_2, is connected in the common-emitter configuration with emitter injection. The second contributing factor to achieving high spurious rejection in the mixer is the constant and "clean" injection voltage across the band. The mixer utilizes the phenomena described by Lotsch[2], whereby the emitter current is selected to minimize third order distortion. The optimum emitter current is a function of the base spreading resistance, r_b', the source resistance, r_s, and the oscillator injection level. Although there is also a frequency dependent parameter, $C_{b'e}$, the optimum current is relatively constant throughout the FM band. In the circuit shown using an SE 5021, this current is approximately 1 mA. Mixer gain is 17 db.

The local oscillator, Q_3, in the common-emitter configuration uses an SE 5022. Its behavior is similar to an over-neutralized amplifier with emitter degeneration. The degeneration eliminates harmonic content in the oscillator waveform. The 100-Ω series collector resistor prevents any common-base mode of operation.

IF AMPLIFIER

The i-f amplifier shown in Fig. 2 uses three identical integrated circuit amplifiers which have been specifically designed for self-limiting applications. Selectivity is obtained with conventional double-tuned interstage filters. The only other components in the i-f amplifier are decoupling capacitors in the supply voltage to each stage.

The bandwidth of each filter is 310 Kc at -3 db with a coupling factor of kQ = 0.8. The overall i-f response including the double-tuned filter at the mixer output is 240 Kc at -6 db and 400 Kc at -45 db. The resulting bandpass, selectivity and phase characteristics of the i-f represent good compromises for stereo multiplex reception.[3]

A single i-f stage with a schematic representation of the integrated circuit amplifier is shown in Fig. 3. The emitter coupled (common-collector feeding common-base) amplifying transistors Q_A and Q_B provide high isolation between input

* Planar is a patented Fairchild process.

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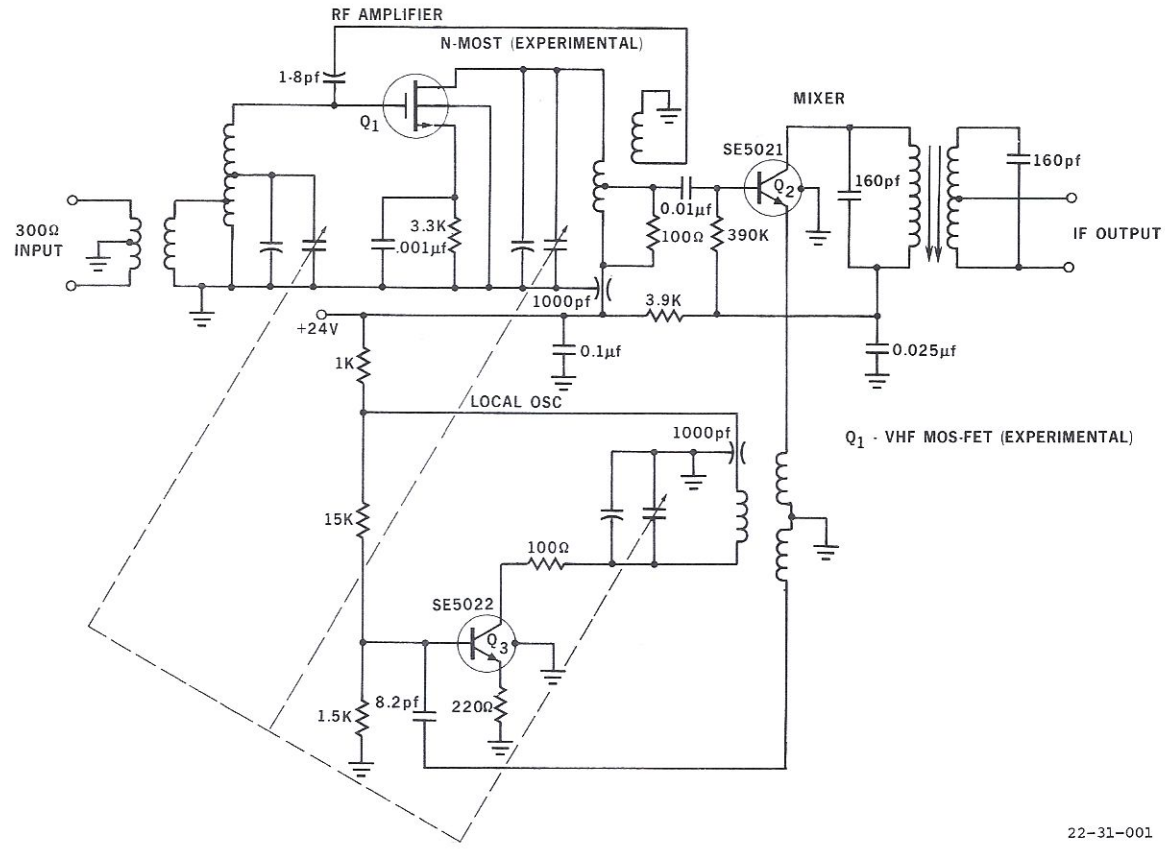

Fig. 1 FM tuner front end

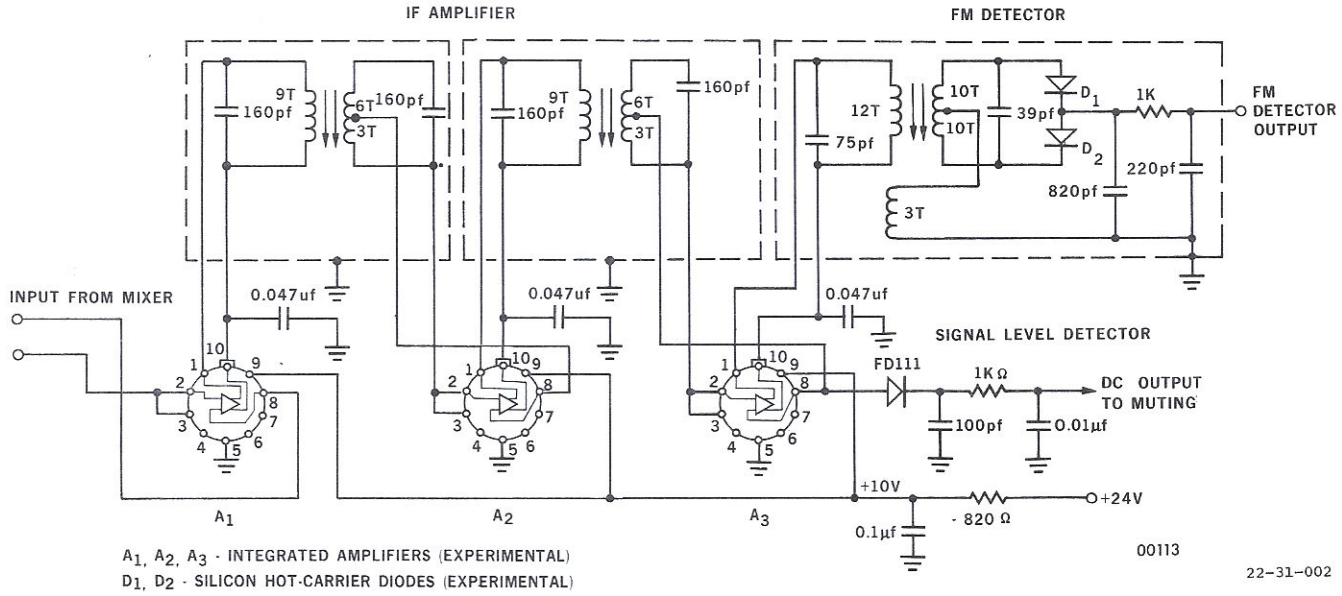

Fig. 2 IF amplifier

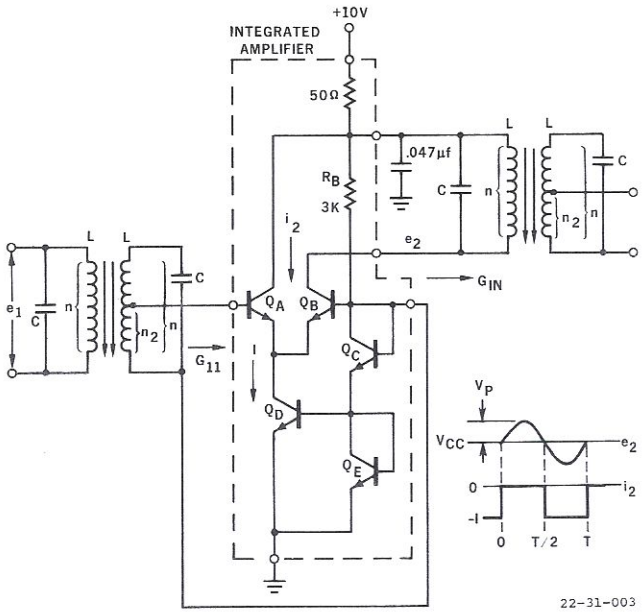

Fig. 3 IF amplifier stage

and output of the integrated amplifier. The bases of Q_A and Q_B are biased above ground by the voltage drop in the two diode-connected transistors, Q_C and Q_E. These transistors, Q_C and Q_E, also form a low impedance AC by-pass to the base of Q_B. The amplifying transistors, Q_A and Q_B, share equal bias current from the current source, Q_D. The current from this source is equal to the current which flows in R_B inasmuch as; (1) the current in R_B flows mainly in the collector of Q_E; (2) the bases of Q_D and Q_E are connected; and (3) Q_D and Q_E have matched V_{BE} and h_{FE} characteristics.

As a small signal amplifier, the common-collector input transistor, Q_A drives the common-base transistor, Q_B. As a large signal amplifier, Q_A can be thought of as a switch which chops the current from Q_D to the emitter of Q_B at the signal frequency rate.

To maintain selectivity, high rejection to AM, low distortion and a good capture ratio in an FM tuner, the band-pass characteristics of the i-f must not be degraded under large signal conditions. To satisfy this requirement in these self-limiting stages, the loading changes on the filters by the integrated amplifiers are minimized by current limiting in Q_B (the collector does not saturate) and mismatching from the filter to the base of Q_A.

Because the common-collector, common-base cascade provides high isolation between input and output, the stability limited gain is extremely high. The self-limiting and band-pass stability properties required in the amplifier impose a gain restriction which is much less than would be the gain based on stability criteria alone. Therefore, except as a second order effect, it was not necessary to consider stability in the design of the i-f amplifier.

The calculated and measured stage gain is about 28 db and is relatively independent of normal spreads which would be expected in the characteristics of the elements within the integrated amplifier.

Detailed i-f design information is contained in the appendix. The actual integrated circuits used in building a prototype to verify the design were more complex than required for this application. These experimental integrated circuits which are discussed in the following section of the paper contain several options to permit feasibility studies for other circuit functions.

INTEGRATED CIRCUIT

General characteristics of integrated components with silicon Planar* technology[4, 5, 6] are summarized in Table 1. This table oversimplifies the design ranges available since it does not specify such interrelations that exist, for example, between f_t in a device and its LV_{CEO}. In fact, a wide variety of possibilities is only resolved when the circuit function required is utilized to place boundary conditions on the problem.

Table 1

INTEGRATED CIRCUIT CHARACTERISTICS

h_{FE}	20-250	±2:1 spread about typical
Δh_{FE} (match)	-	±25%
ΔV_{BE} (match)	-	±2 mV typical
BV_{CBO}	20-100 V	
LV_{CEO}	15-60 V	
f_t	0.3-1 Gc	
R	10 Ω-100 K	±25%
ΔR (match)	-	±5%

The integrated circuit in the i-f strip was fabricated using diffused isolation junctions to electrically separate the components. A cross-sectional illustration of the Planar* process utilized and the resulting devices are shown in Fig. 4. The anode of the isolation diode which is a parasitic element is placed at the most negative potential in the circuit.

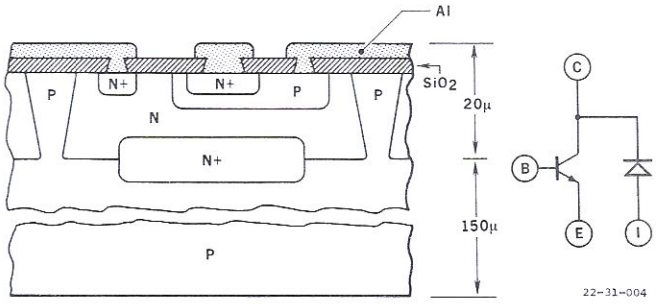

Fig. 4 Integrated transistor with P-N junction isolation

A photograph of the complete integrated circuit and its schematic representation is shown in Figs. 5 and 6. Several circuit configurations are realizable with this one circuit which has self-contained bias networks included. For FM i-f amplifications, the integrated circuit is connected in the emitter-coupled amplifier configuration shown in Fig. 2.

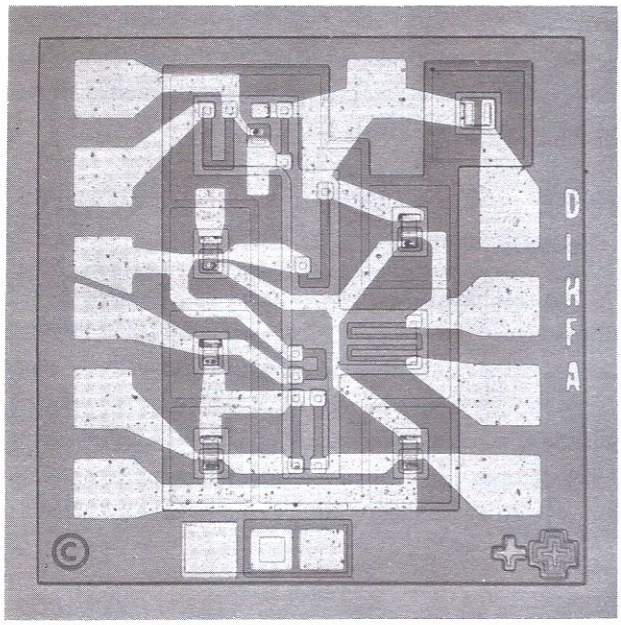

Fig. 5 Photomicrograph of experimental integrated circuit

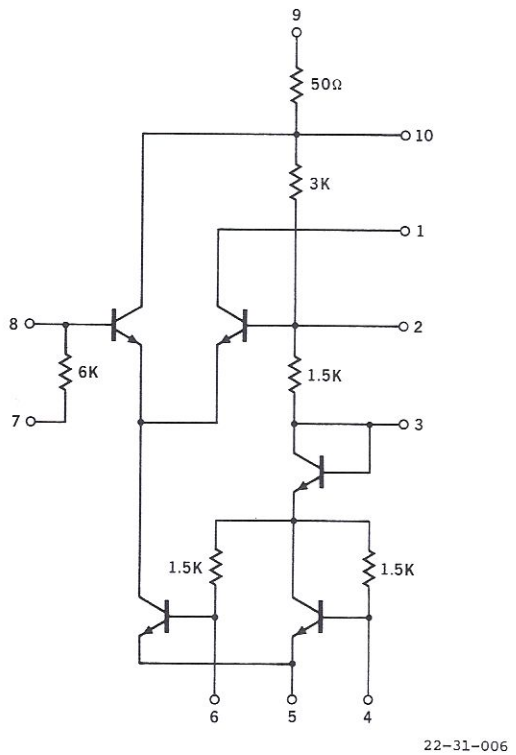

Fig. 6 Experimental integrated circuit

Other connections have been investigated for AM i-f amplifiers with AGC, mixer-oscillators and video amplifiers. Typical "Y" parameters of the emitter-coupled configuration are given in Table 2.

Table 2

TYPICAL MEASURED "Y" PARAMETERS OF THE EMITTER-COUPLED INTEGRATED CIRCUIT AMPLIFIER

Conditions: V_{CC} = +10 V, f = 10.7 Mc

Y_{11} = 0.7 mmhos ∠ 37° (G_{11} = 0.56 mmhos, C_{11} = 6 pf)
Y_{12} = 5 μmhos ∠ -90° (C_{12} = 0.07 pf)
Y_{21} = 21 mmhos ∠ 170°
Y_{22} = 0.2 mmhos ∠ 85° (G_{22} = 0.02 mmhos, C_{22} = 3 pf)

FM DETECTOR

The FM detector shown in Fig. 2 is a modification of the conventional ratio detector originally described by Seeley and Avins.[7] The important difference is the absence of the rc network associated with the detector diodes. In this simplified detector configuration, the forward voltage drop of the two silicon detector diodes is utilized to replace the voltage offset normally developed across a large electrolytic capacitor in the rc network of the conventional ratio detector.

The circuit has not been analyzed in detail but test results of an empirical design are very encouraging. Experimental silicon hot carrier diodes with a 0.6-volt forward drop and 0.5-pf capacitance at zero bias gave best detector performance. Conventional silicon junction diodes resulted in slightly increased detector distortion at very low input levels. One inherent disadvantage of the detector is its low output. In this design the output is 250 mV peak-to-peak for ±75 Kc deviation. However, aside from this minor limitation, the detector appears to have excellent capabilities. Its performance could almost certainly be further improved with additional design effort.

MUTING AND TUNING INDICATOR

Muting circuitry shown in Fig. 7 automatically places the multiplex decoder in monophonic operation on weak stereo stations. On very weak stations and for interstation noise, it completely mutes the output from the FM detector.

The rectified output of the last i-f filter operates the signal strength tuning meter and is amplified to drive the stereo killer transistor and MOS-FET muting switch. The stereo killer operates for tuner inputs less than 50 μV. Below 30 μV, muting comes in unless defeated by the muting "ON-OFF" switch.

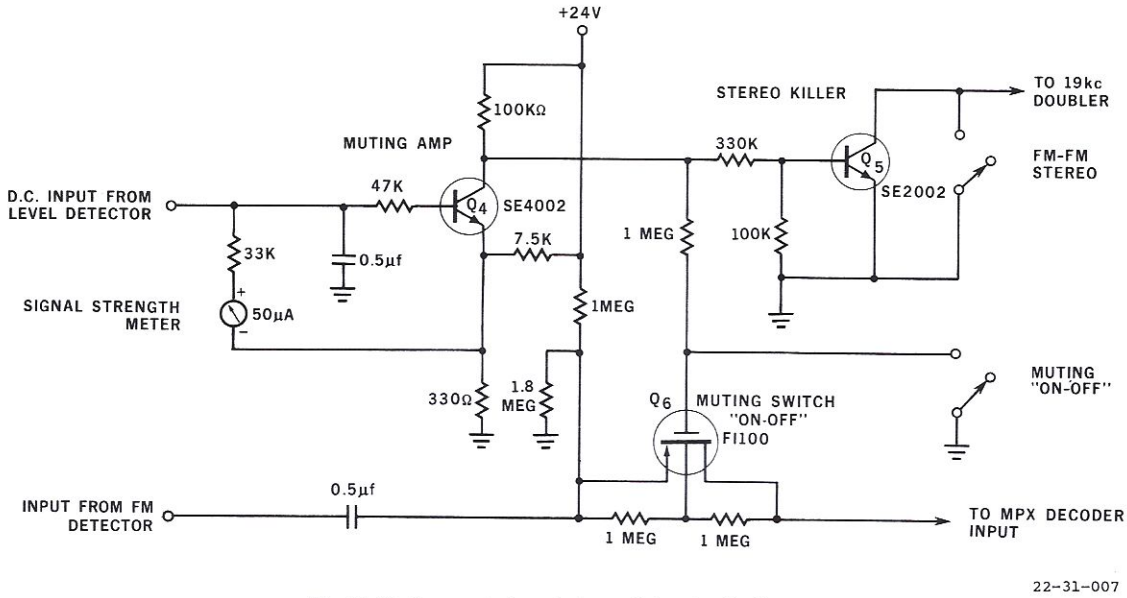

Fig. 7 Muting and signal strength tuning indicator

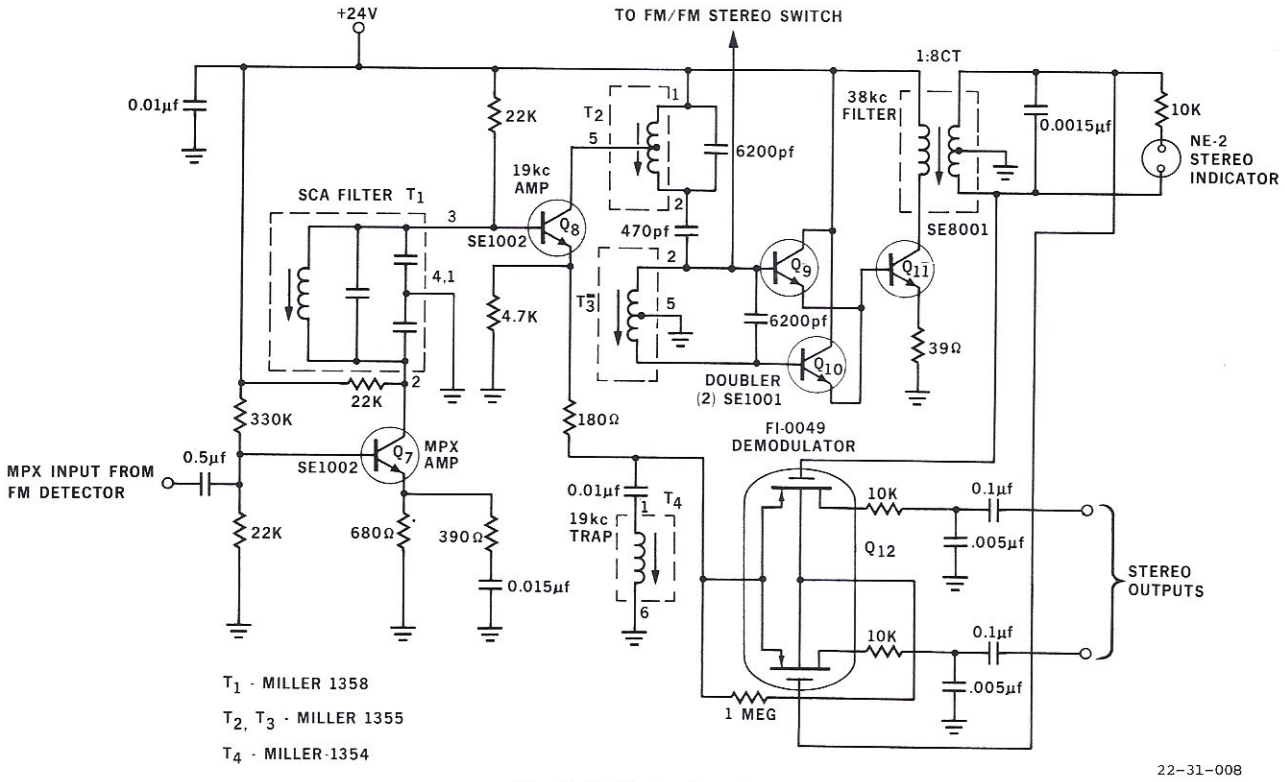

Fig. 8 Multiplex decoder

MULTIPLEX DECODER

The multiplex decoder shown in Fig. 8 demodulates the composite signal from the FM detector. With the maximum 250 mV peak-to-peak input level from the FM detector, the corresponding output level of the decoder is 0.8 V rms. The decoder has automatic stereo-monophonic mode selection with a light indicating stereo operation. On weak stereo stations the decoder is placed in monophonic operation by a stereo killer to obtain the best possible signal-to-noise ratio. With a manual "FM-FM STEREO" switch, it is possible to place the decoder in monophonic operation for all received signals.

The input transistor, Q_7, amplifies the composite signal and accentuates the multiplex subcarrier frequency components (23 Kc to 53 Kc) to the degree necessary to have high separation in a switching type demodulator. A rejection filter in the collector of Q_7 removes SCA information from the composite signal.

The second amplifier, Q_8, serves as a low impedance drive to the demodulator and also removes the 19 Kc pilot from the multiplex signal. Two 19 Kc filters, a single and a double-tuned, provide high rejection to audio and subcarrier frequencies, thus eliminating any significant phase modulation of the extracted 19-Kc pilot by these adjacent frequencies.

The 19-Kc output of the double-tuned filter is doubled in Q_9 and Q_{10} which feed the base of the 38-Kc amplifier, Q_{11}. The output of the 38-Kc transformer drives the gates of the dual MOS-FET device, Q_{12}, which operates as two switches to demodulate the multiplex signal. The neon lamp has two functions. It indicates stereo operation and it limits the amplitude of the MOS-FET gate drive. The de-emphasis networks at the demodulator outputs provide sufficient attenuation to the 38-Kc switching frequency to alleviate the need for additional 38-Kc filtering.

In the absence of the 19-Kc pilot in the composite signal from the tuner (monophonic reception) or if the 19-Kc pilot is by-passed to ground either by the "FM-FM STEREO" switch or the stereo killer, there is no 38-Kc signal at the gates of the demodulator, Q_{12}. In this monophonic mode of operation, the demodulator, Q_{12}, is on continuously and the multiplex decoder is merely an audio amplifier with two identical de-emphasized outputs.

POWER SUPPLY

The unregulated +24-V supply for the FM tuner shown in Fig. 9 uses a single transistor, Q_{13}, in a ripple-reduction circuit.

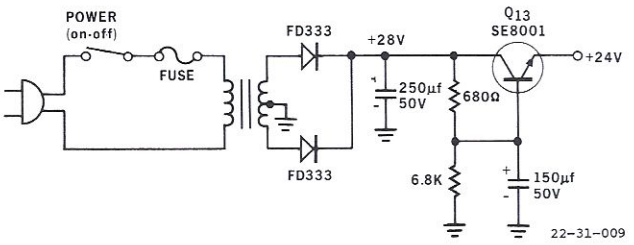

Fig. 9 Power supply

PERFORMANCE

The performance of the tuner is given in Table 3. Most of the measurements are based on IHF standards.

CONCLUSION

Although the MOS-FET r-f amplifier shows considerable improvement over bipolar transistors in overload capabilities and rejection of spurious responses, further device improvements promise even better performance. Since the initiation of this project, the Fairchild Research and Development Laboratories have fabricated devices with 15-db gain and 3-db noise figure at 400 Mc; and 20-db gain and 2-db noise figure at 200 Mc.

Table 3

TUNER PERFORMANCE

30 db Usable Sensitivity	3 µ V
Signal-to-Noise Ratio	65 db
Alternate Channel Selectivity	30 db
Peak-to-Peak FM Detector Separation	800 Kc
Capture Ratio	1 db
AM Rejection	40 db
Detector Frequency Response	65 Kc
1 Kc Total Harmonic Distortion	0.6%
Image Rejection	35 db
i-f Rejection	60 db
Spurious Response Rejection	80 db
Oscillator Drift, 105 to 125 VAC	20 Kc
Multiplex Separation	25 db
Multiplex Output	0.8 V

Integrated circuits can now perform a variety of linear functions using improved technology which incorporates such processes as thin-film resistors, high-frequency transistors, field-effect devices and dielectric isolation on a compatible monolithic chip of silicon. The integrated self limiting FM i-f amplifiers described in the paper are well within the current state of the art. These amplifiers have improved performance over conventional FM i-f stages and can be offered at a cost which is competitive with discrete i-f amplifier components. Overall i-f costs with integrated devices would be lower because of simplified assembly.

The development of new devices such as those discussed in this paper calls for ever-increasing cooperation between the set manufacturer and the device manufacturer. The results of these joint efforts will ultimately lead to better and less expensive entertainment products for the consumer.

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APPENDIX

Design of 10.7-Mc I-f Amplifier

The i-f filters are designed to achieve the desired overall amplitude and phase responses with maximum stage gain while working within the restrictions of having self-limiting action and stable bandpass characteristics under all signal conditions.

A single i-f stage is shown in Fig. 3. Filter loading by the amplifier input is made small and the variations minimized by mismatching from the filter to the amplifier input. This mismatch is expressed as a ratio, R, of unloaded to loaded Q.

$$\frac{Q_{coil}}{Q_{LS}} = R \tag{1}$$

With identical primary and secondary filter coils, this ratio also relates primary loaded Q to secondary loaded Q since the primary coil has negligible loading by the amplifier. Thus,

$$\frac{Q_{PL}}{Q_{SL}} = R \tag{2}$$

As a compromise between bandshape stability and gain, a mismatch is arbitrarily selected to cause a 20% reduction in the Q of the secondary coil when loaded by a typical small-signal amplifier input impedance.

From this,

$$\frac{Q_{coil}}{Q_{LS}} = \frac{Q_{PL}}{Q_{SL}} = R = 1.25 \tag{3}$$

The bandpass and phase response of the i-f is determined by the loaded Q of the primary and secondary coils and by the coupling factor.

For equal loaded Q coils, bandwidth and Q are related by

$$Q_L = \frac{Kf}{BW_{3\,db}} \tag{4}$$

where K depends on the coupling factor and f is the i-f frequency. A coupling factor, kQ = 0.8 with a 3-db bandwidth of 310 Kc for each filter results in a desirable overall i-f response.[3] For kQ = 0.8; K = 0.96 and the load Q is

$$Q_L = 39 \tag{5}$$

The bandpass characteristics for nearly equal loaded primary and secondary Q coils is given by equation (4) with sufficient accuracy when Q_L is expressed as

$$Q_L = \sqrt{Q_{PL}\,Q_{SL}} \tag{6}$$

Therefore, for the desired i-f response

$$\sqrt{Q_{PL}\,Q_{SL}} = 39\,, \tag{7}$$

$$Q_{PL} = Q_{coil} = 44 \tag{8}$$

and

$$Q_{SL} = 35 \tag{9}$$

Filter loading by the amplifier output is prevented by limiting without saturation. The proper load termination (filter input admittance) which satisfies this requirement is established in the following analysis.

At full limiting the power delivered into the filter is

$$P_L = \frac{V_p^{\,2} G_{IN}}{2} \tag{10}$$

where V_p is the peak voltage swing on the collector of Q_2 and G_{IN} is the filter input admittance at resonance.

The power from the output stage, Q_2, is

$$P_o = \frac{1}{T}\int_o^T e_2 i_2\, dt \tag{11}$$

where, referring to Fig. 3, T is the period for one cycle,

$$e_2 = V_p \sin \frac{2\pi}{T} t\,, \tag{12}$$

$$i_2 = 0 \text{ for } 0 < t < \frac{T}{2} \tag{13}$$

and

$$i_2 = -I \text{ for } \frac{T}{2} < t < T \tag{14}$$

Therefore,

$$P_o = \frac{1}{T}\int_{\frac{T}{2}}^{T} V_p \sin \frac{2\pi}{T} t\,(-I)\, dt \tag{15}$$

Integrating,

$$P_o = \frac{V_p I}{\pi} \tag{16}$$

Equating P_L and P_o, and solving for G_{IN},

$$G_{IN} = \frac{2I}{\pi V_p} \tag{17}$$

For the described nearly equal primary and secondary Q filters with kQ = 0.8, the input conductance is given by the approximation

$$G_{IN} \simeq 1.5\, g_c \tag{18}$$

where g_c, the equivalent parallel conductance of the filter coils, is given by

$$g_c = \frac{1}{2\pi f L\, Q_{coil}} \tag{19}$$

Solving equations (17), (18), and (19) for the required coil inductance L in terms of Q_{coil}, f, I, and V_p gives

$$L = \frac{3 V_p}{8 f I Q_{coil}} \tag{20}$$

To ensure that Q_2 will operate well out of saturation with expected tolerances in filter and integrated amplifier characteristics, V_p is made one-half of the supply voltage, V_{CC}.

Thus,

$$L = \frac{3\, V_{CC}}{16 f I Q_{coil}} \tag{21}$$

The current I is given by

$$I = \frac{V_{CC} - V_{BE(C)} - V_{BE(E)}}{R_B} \tag{22}$$

For V_{CC} = 10 V, $V_{BE(C)} = V_{BE(E)}$ = 0.7 V and R_B = 3 KΩ,

$$I = 2.9 \text{ mA} \tag{23}$$

and

$$L = 1.4\ \mu\text{h} \tag{24}$$

The resonating capacitor, C, is

$$C = \frac{1}{4\pi^2 f^2 L} = 160 \text{ pf} \tag{25}$$

Coil conductance, g_c, is

$$g_c = 2.4 \times 10^{-4}\ \mho \tag{26}$$

and the filter input conductance is

$$G_{IN} = 3.6 \times 10^{-4}\ \mho \tag{27}$$

The turns ratio, $\frac{n}{n_2}$, to give the desired mismatch from the filter output to the amplifier input can now be determined;

$$\frac{Q_{coil}}{Q_{LS}} = \frac{G_{11}}{\left(\frac{n}{n_2}\right)^2 g_c} + 1 \tag{28}$$

where G_{11} is the typical small signal input conductance of the amplifier. Based on hybrid -π equivalent circuits for Q_1 and Q_2, G_{11} is given by

$$G_{11} \simeq \frac{1}{2 r_e h_{fe}} \tag{29}$$

where

$$r_e = \frac{kT}{q\frac{I}{2}} \tag{30}$$

For I = 2.9 mA, the value of r_e at room temperature is 18 ohms. With a typical h_{fe} of 50,

$$G_{11} = 5.6 \times 10^{-4}\ \mho \tag{31}$$

Solving equations (3), (26), (28), and (31) for $\frac{n}{n_2}$,

$$\frac{n}{n_2} = 3.1 \tag{32}$$

The small signal gain of a stage, referring to Fig. 3, is defined as

$$A_v^2 = A_p \triangleq \left(\frac{e_2}{e_1}\right)^2 \tag{33}$$

The voltage ratio, $\frac{e_2}{e_1}$, is given by

$$\frac{e_2}{e_1} \simeq \frac{Y_f}{G_{IN}\left(\frac{n}{n_2}\right)} \tag{34}$$

where Y_f is the forward transfer admittance. From Hybrid -π equivalent circuits for Q_1 and Q_2 it can be shown that

$$Y_f \simeq \frac{qI}{4kT} \tag{35}$$

and at room temperature, for I = 2.9 mA,

$$Y_f = 2.8 \times 10^{-2}\ \mho \tag{36}$$

Solving for $\frac{e_2}{e_1}$ from equations (17), (32), (34), and (36)

$$\frac{e_2}{e_1} = 25 \tag{37}$$

Squaring this ratio, the stage gain is

$$A_v^2 = A_p = 625 \text{ (28 db)} \tag{38}$$